In the Specification:

Please amend paragraph [0020] as follows:

In operation, the memory cell forms two complementary nodes, node-1 and node-2. Because node-1 is tied to the gate of the second pull-up transistor ~~PG-2~~ PU-2 and node-2 is tied to the gate of the first pull-up transistor ~~PG-1~~ PU-1, the values stored in each node will remain complementary to each other. For example, when node-1 is high, the PMOS second pull-up transistor PU-2 prevents the current from the current source V_{cc} from flowing to node-2. In parallel, the gate of the NMOS second pull-down transistor PD-2 is activated, allowing any charge that may be in node-2 to go to ground. Furthermore, when node-2 is low, the PMOS first pull-up transistor PU-1 allows current to flow from V_{cc} to node-1, and the gate of the NMOS first pull-down transistor PD-1 is de-activated, preventing the charge in node-1 from going to ground. The gates of the first pass-gate transistor PG-1 and the second pass-gate transistor PG-2 are electrically coupled to a word line (WL) to control reading data from and writing data to the memory cell. Values stored in node-1 and node-2 are read on a bit-line (BL) and a complementary-BL, respectively, which are electrically coupled to a sense amplifier (not shown).

Please amend paragraph [0027] as follows:

The source of the second pass-gate transistor PG-2 is electrically coupled to the complementary-BL via a complementary-BL contact line 236 and plug 237. Similarly, the second pass-gate transistor PG-2 electrically couples the BLB to the drain of the second pull-up transistor PU-2 and the drain of the second pull-down transistor PD-2. The gate of the second pass-gate transistor PG-2 is electrically coupled to the WL via a

WL contact line 238 on M1 and plug 239. One of ordinary skill in the art will appreciate that the above structure defines a unit or memory cell 260, as illustrated by the dotted line. The unit cell 260 defines the basic building block for designing memory cells and may be duplicated to create larger memories. In the preferred embodiment, the length of the longer side of the unit cell 260 is about 2 times or greater the length of the shorter side of the unit cell 260. Moreover, it is preferred that the length of the shorter side of the unit cell 260 is about 0.485 μm or shorter. In the preferred embodiment, the transistors are aligned such that the longitudinal axis of the source/drain regions are parallel to the shorter side of the unit ~~cell 160~~ cell 260.

Please amend paragraph [0037] as follows:

Regarding the complementary-BL 340, a via 342 electrically couples the complementary-BL 340 on M3 to contact line 344 on M2, which is electrically coupled to contact line 236 on M1 through via 346. The contact line 236 on M1 is electronically coupled to the source of the second ~~pull~~ pass-gate transistor ~~PG-1 as~~ PG-2 as discussed above with reference to FIG. 2.

Please amend paragraph [0038] as follows:

Regarding the second V_{ss} line 350, a via 352 electrically couples the V_{ss} line 350 on M3 to contact line 354 on M2, which is electrically coupled to contact line 230 on M1 through via 356. The contact line 230 on M1 is electricallly coupled to the source of the second pull-down transistor ~~PD-1 as~~ PD-2 as discussed above with reference to FIG. 2.